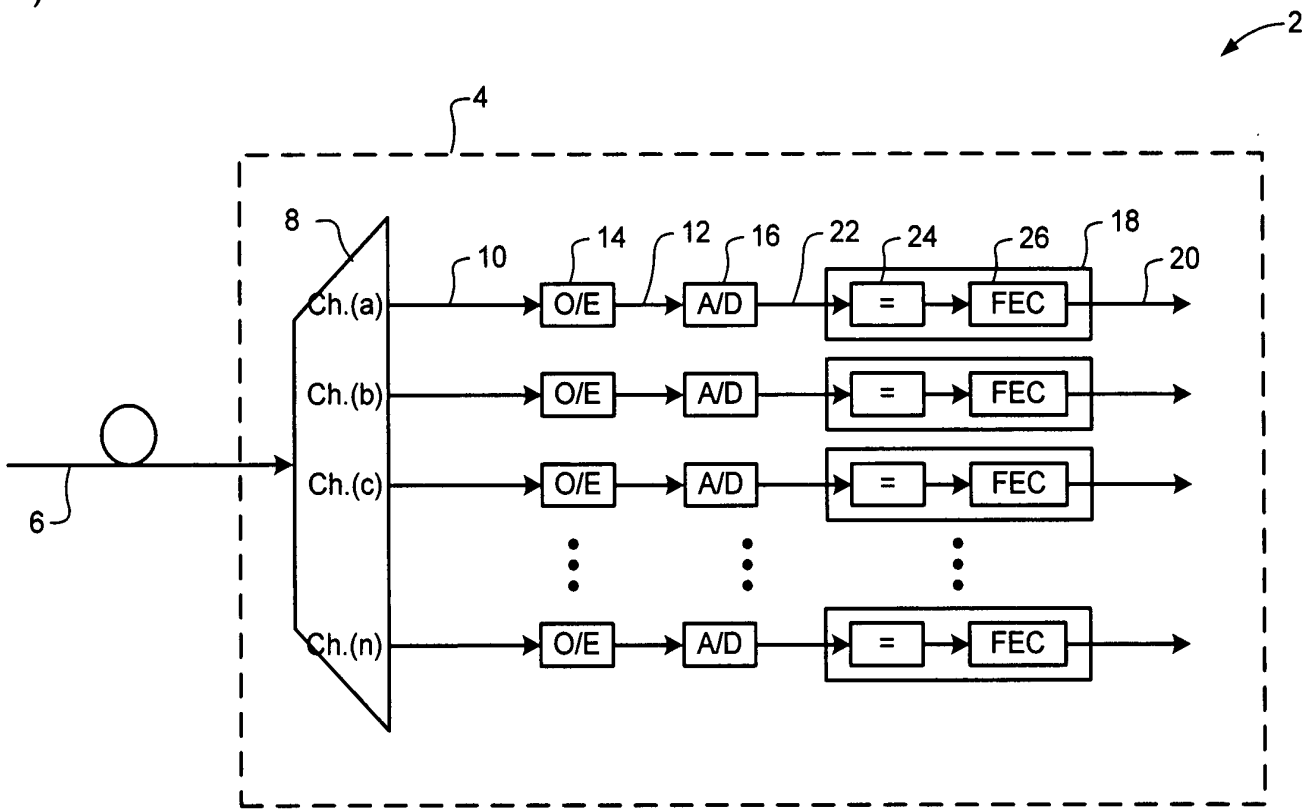
Figure 1
(Prior Art)



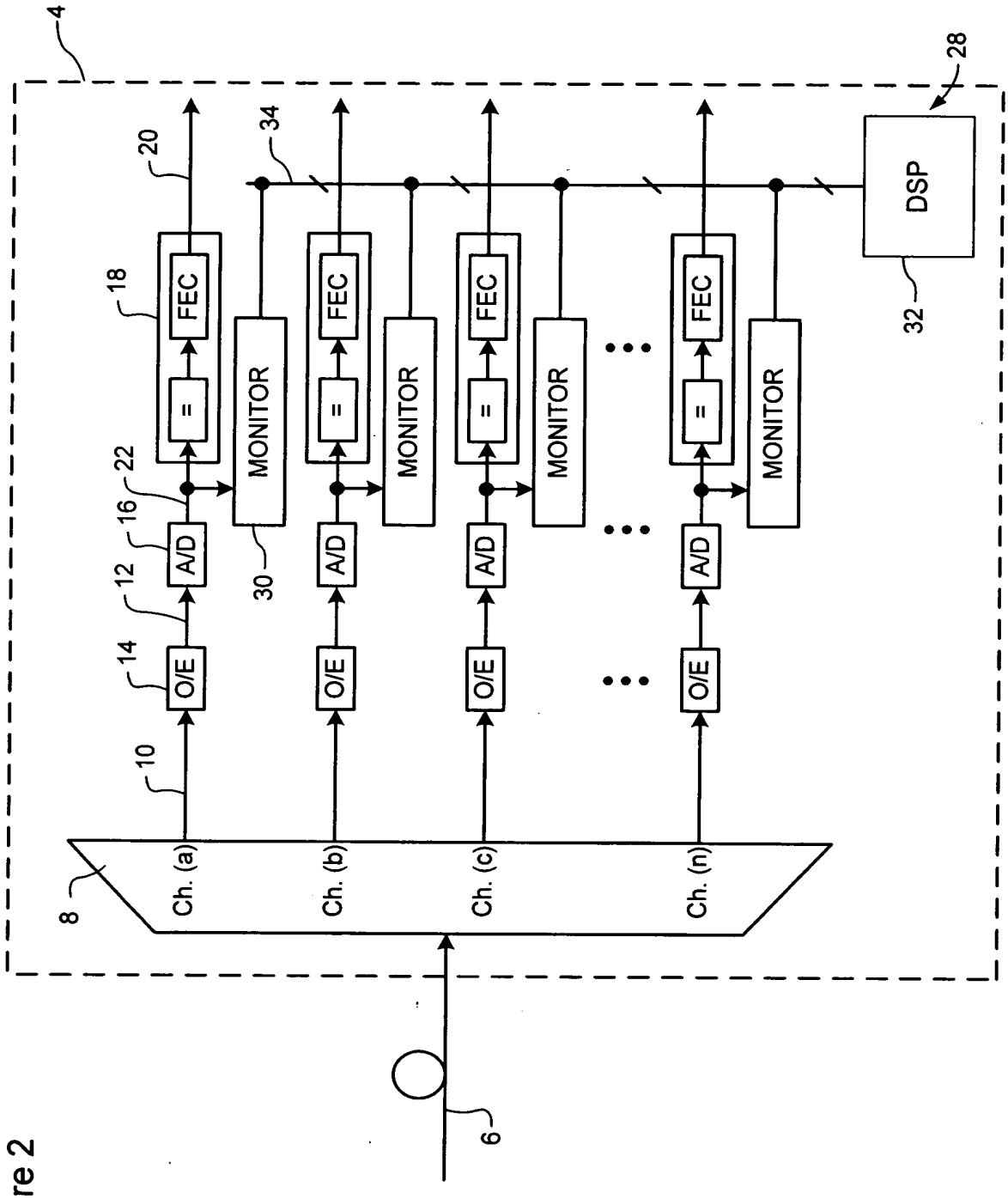

4
28
DSP
32
34
20
18
FEC
=
22
16
MONITOR
30
12
A/D
14
O/E
10
8
Ch. (a)
Ch. (b)
Ch. (c)
Ch. (n)
6

Figure 2

Figure 3

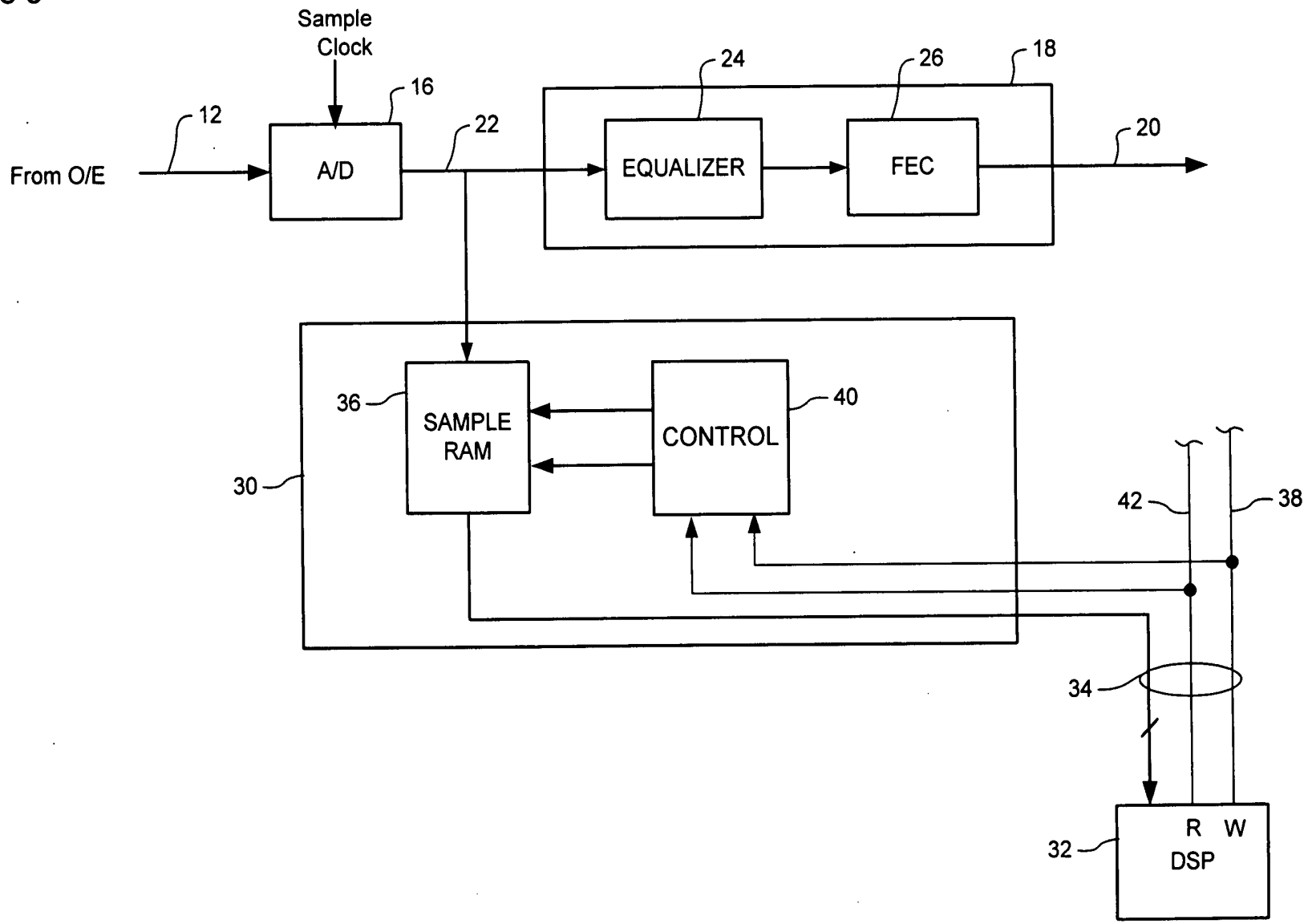

Sample
Clock
16
12
From O/E
A/D
22
24
26
18
EQUALIZER
FEC
20
36
SAMPLE
RAM
CONTROL
40
30
42
38
34
R W
DSP
32

Figure 4

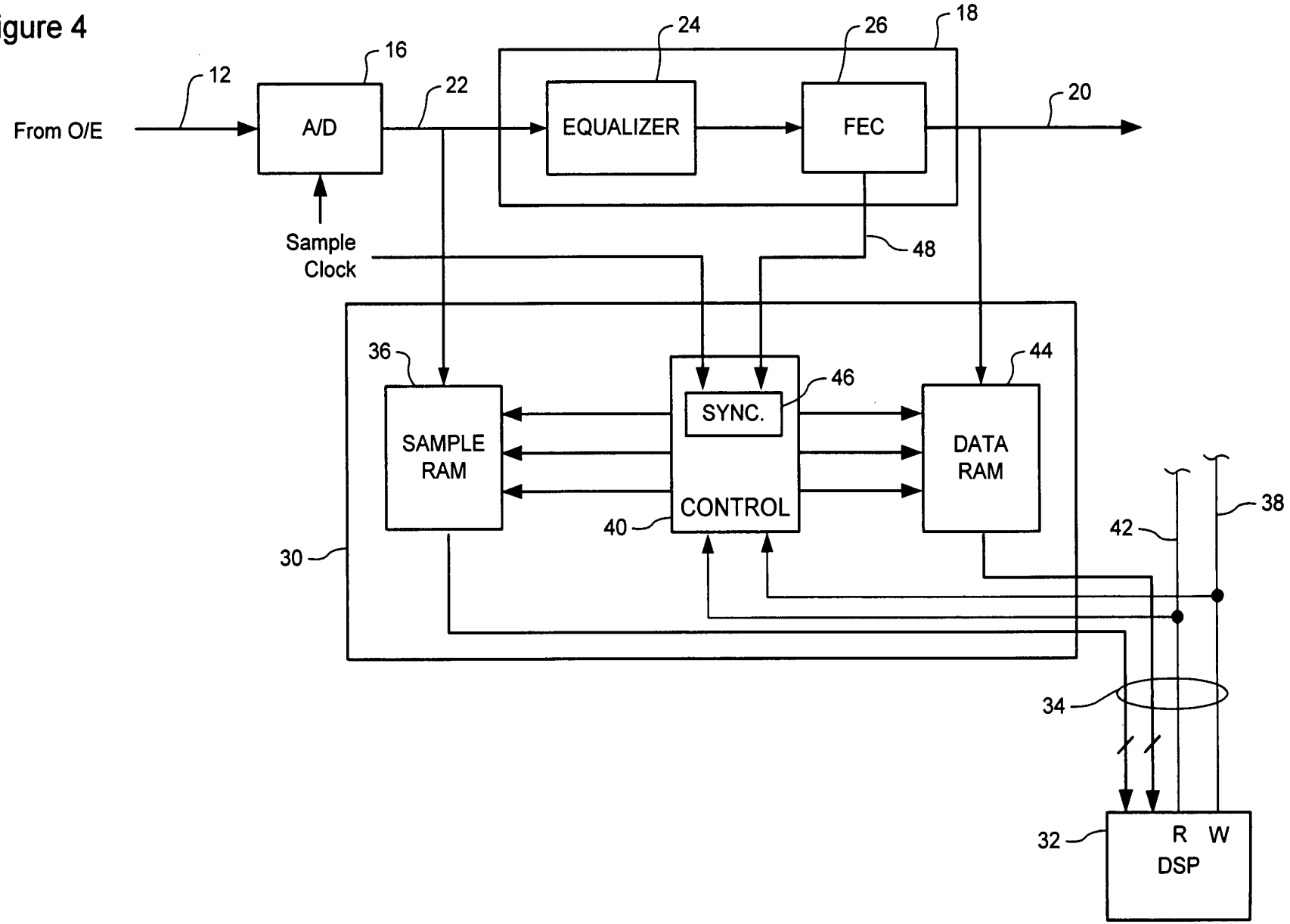

From O/E
12
A/D
16
22
EQUALIZER
24
FEC
26
18
20
Sample Clock
48
36
SAMPLE RAM
SYNC.
46
CONTROL
40
DATA RAM
44
30
42
38
34
32
R W
DSP

Figure 5a

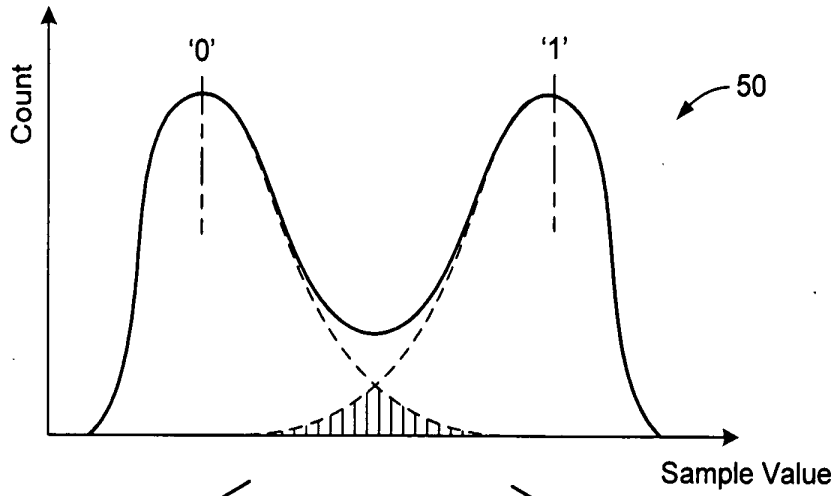


Figure 5b

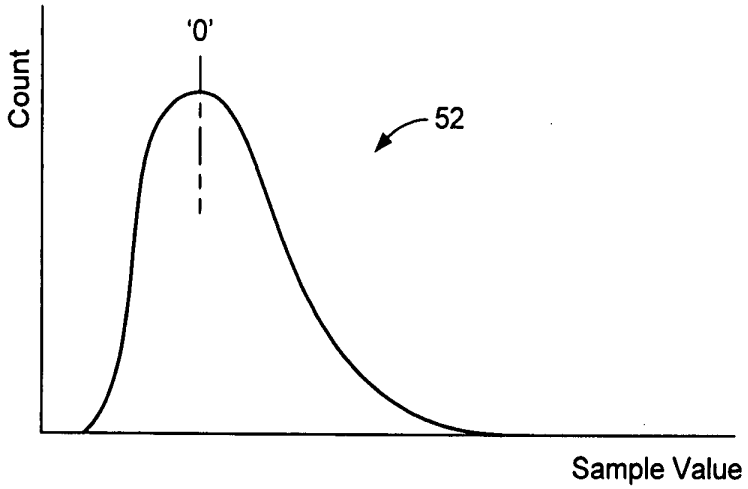


Figure 5c

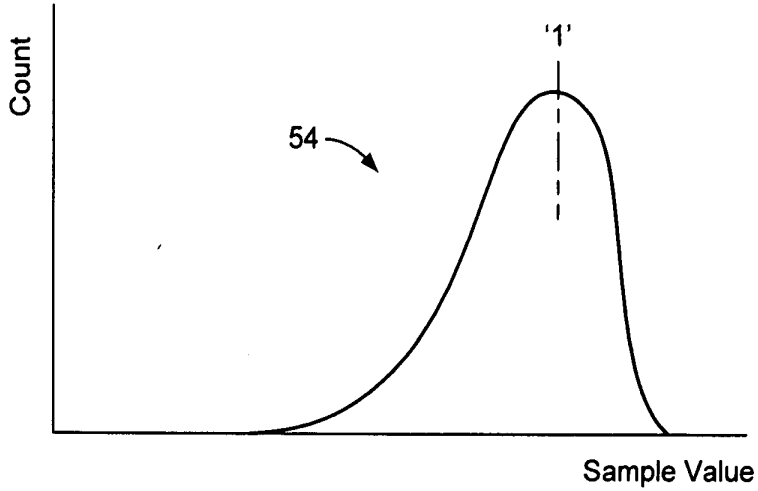
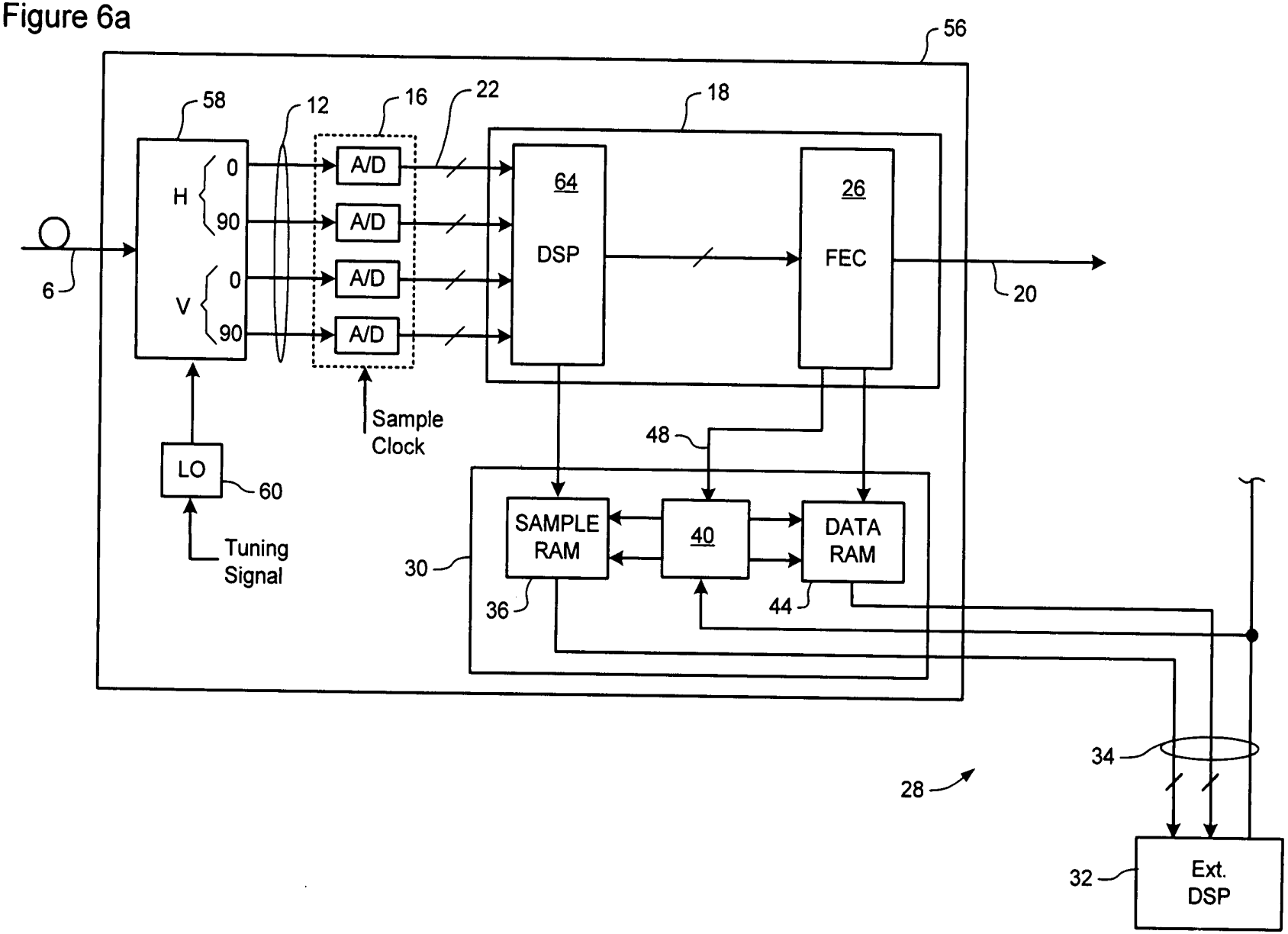


Figure 6a


56
58
12
16
22
18
H
0
90
V
0
90
A/D
A/D
A/D
A/D
64
DSP
26
FEC
6
20
Sample
Clock
48
LO
60
Tuning
Signal
SAMPLE
RAM
40
DATA
RAM
30
36
44
34
28
32
Ext.
DSP

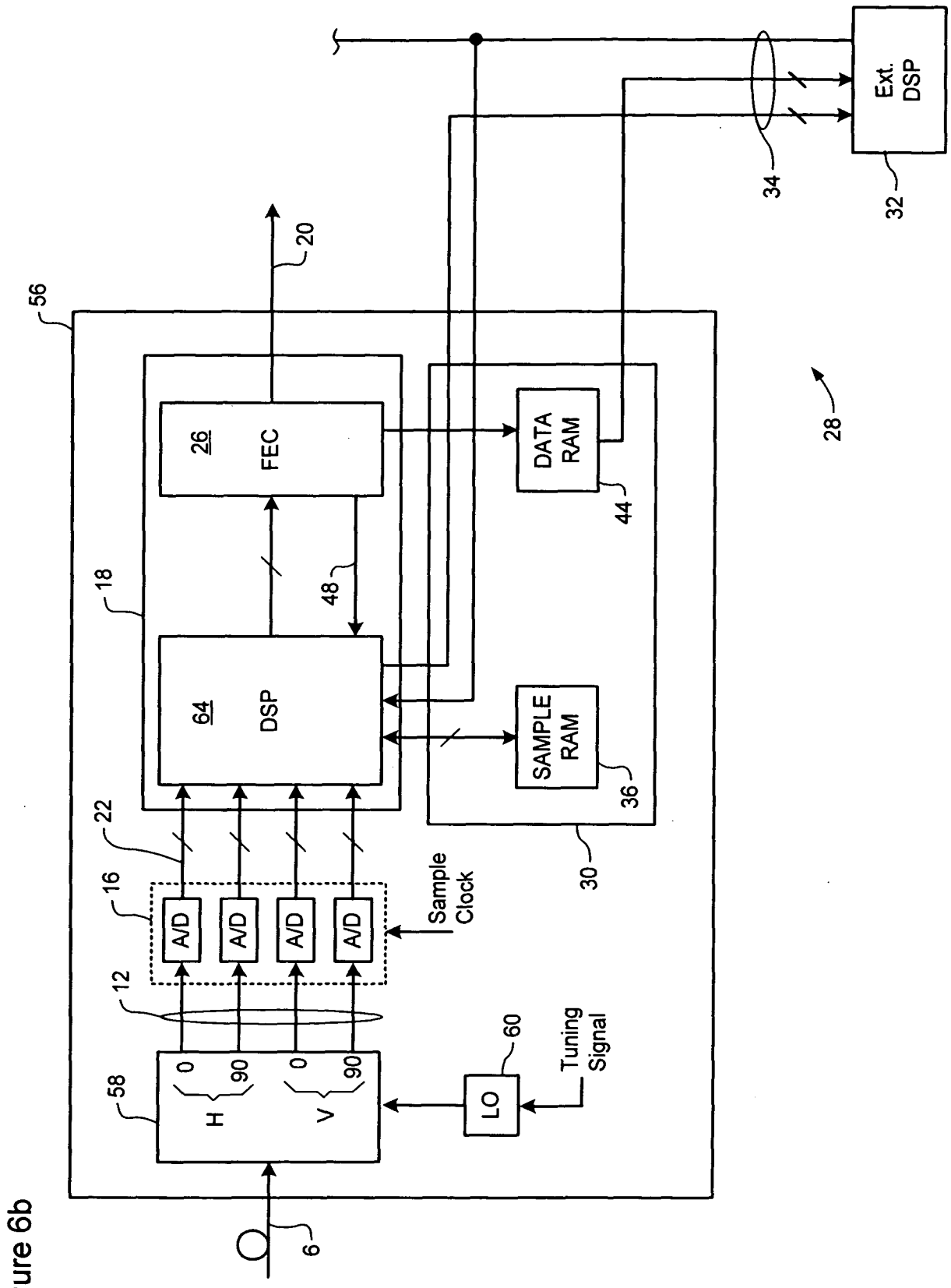

Ext. DSP
34
32
28
56
20
26 FEC
DATA RAM
44
18
48
64 DSP
SAMPLE RAM
36
30
22
16
A/D
A/D
A/D
A/D
Sample Clock
12
58
0
90
H
0
90
V
LO
60
Tuning Signal
6

Figure 6b

Figure 7

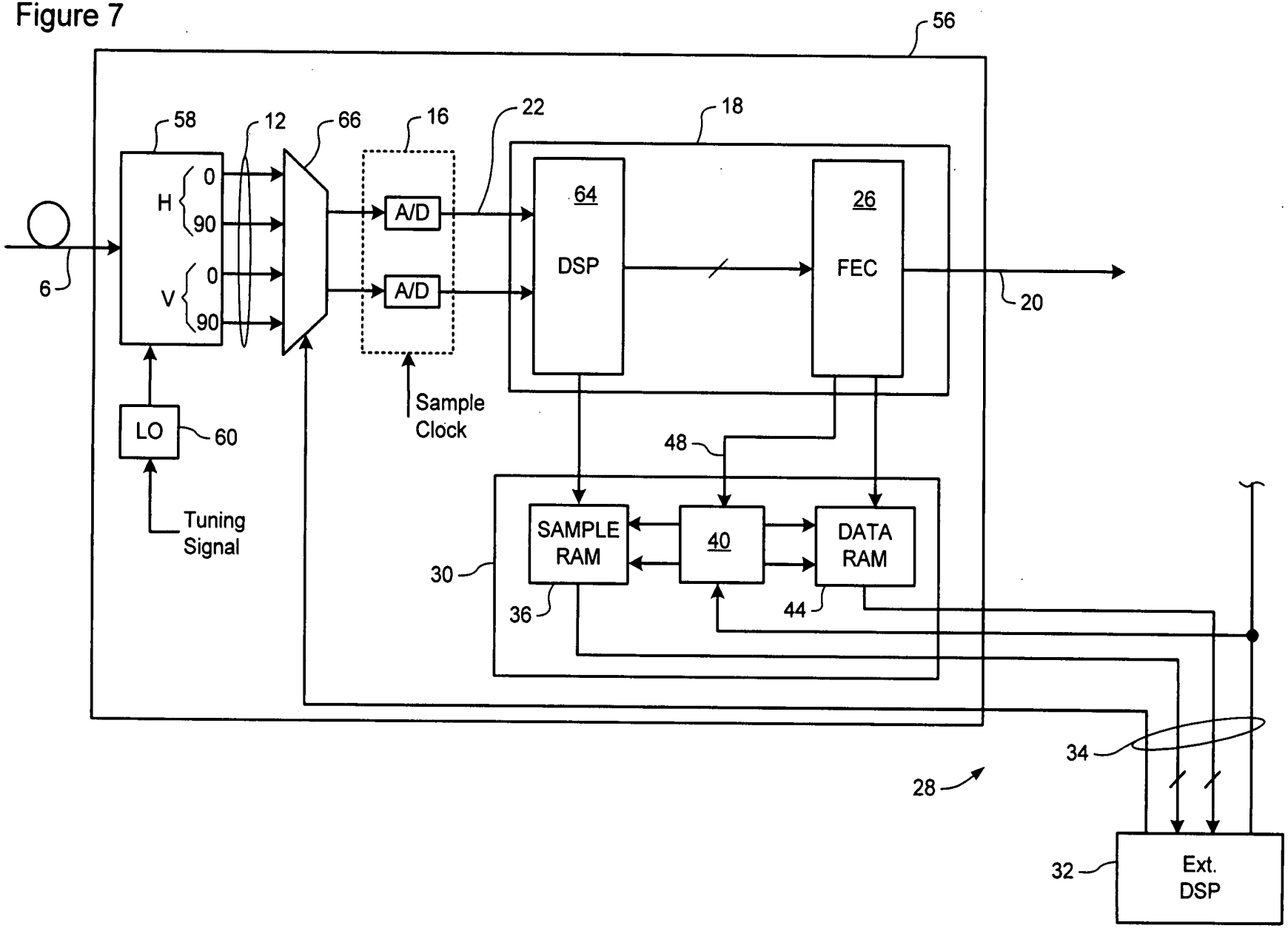
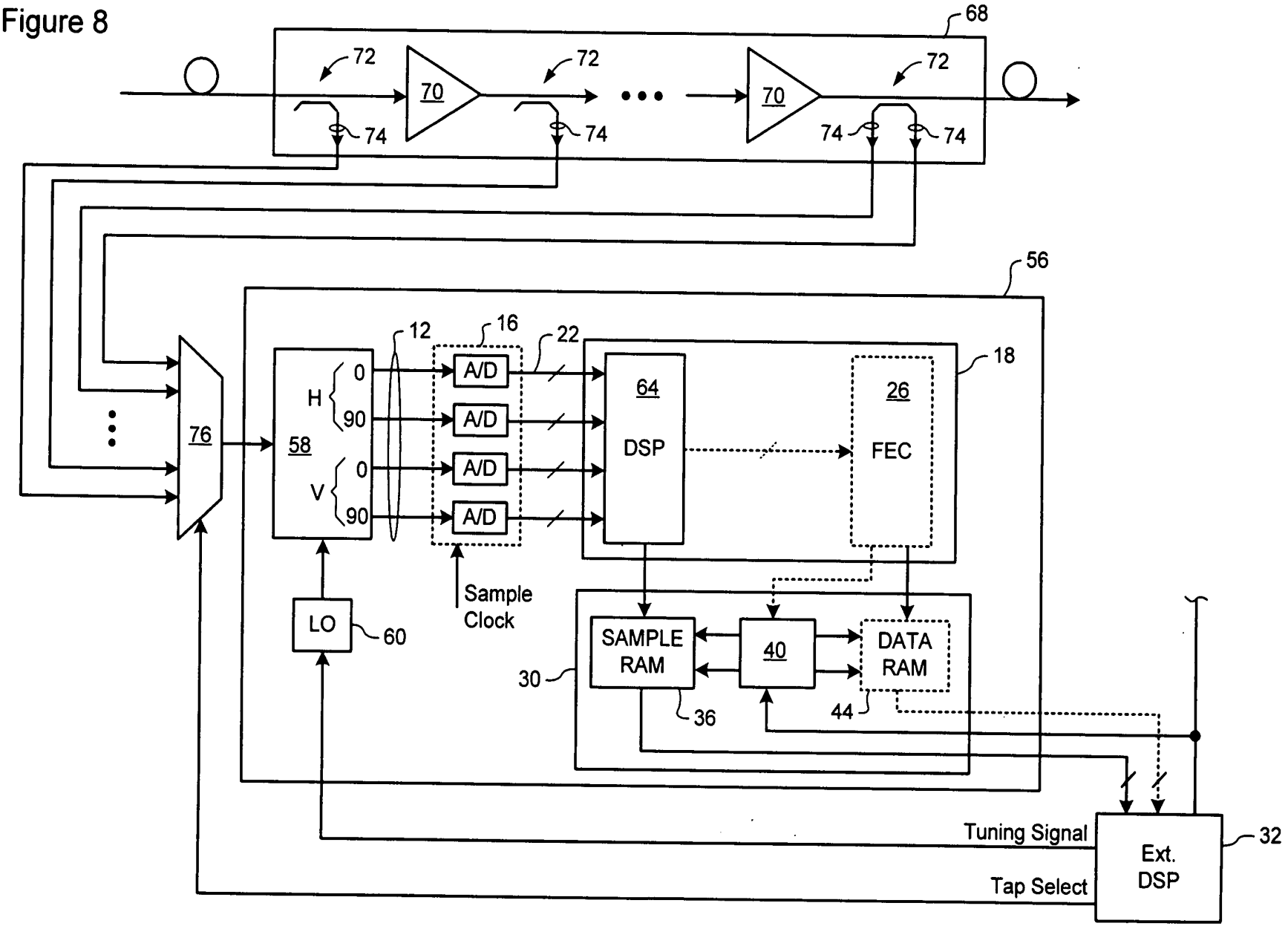

56
58
12
66
16
22
18
H
0
90
V
0
90
A/D
A/D
64
DSP
26
FEC
6
20
LO
60
Tuning
Signal
Sample
Clock
48
SAMPLE
RAM
40
DATA
RAM
30
36
44
34
28
32
Ext.
DSP

Figure 8


68
72
70
74
56
12
16
22
18
76
58
H
V
0
90
A/D
64
DSP
26
FEC
LO
60
Sample
Clock
SAMPLE
RAM
30
40
DATA
RAM
36
44
Tuning Signal
Tap Select
Ext.
DSP
32